KEITHLEY

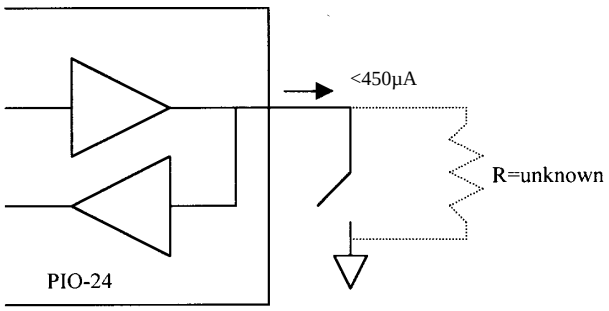
PIO-24 Product Change Notice

Packing List

Description

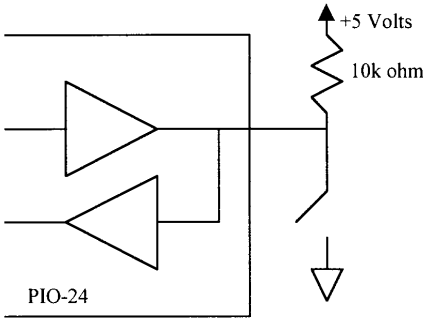
Due to a component change implemented in March 1999, the input load current of the PIO-24 digital I/O card was reduced and made more consistent. The input load current on the newly designed board is now ≤-2µA, which continues to meet the product specification of ≤-450µA. This change was made because some devices having low drive current, such as the ERB-24, were accidentally being turned on when power was first applied to the PIO-24 (the specific change involved changing parts U3, U6, and U9, the digital input latches). The older design used 74LS373 octal tri-state latches, which had a higher input load current than the 74HCT373 parts that are now being used. In existing designs using the PIO-24, this reduction in input load current will generally cause no problems. However, if the existing design depends on this input load current being near the -450µA limit, this change is important. The reduction in input load current means that the input state will be much less likely to be driven high if the input is floating. Figure 1 shows an application monitoring a contact switch that would be a problem as a result of the new design, and Figure 2 shows the correct implementation of this application that would work with either design.

Figure 1
Poor implementation of monitoring a digital input



In Figure 1, the digital input would most likely float high with an older design board because of the higher input load current. When the switch is closed, the input will be pulled low. While this would work on an older design of the PIO-24, this is a poor implementation because the input load current can vary from one board to the next. In the case of a new design board, this would not work because of the lower load current.

Figure 2
Better implementation of monitoring a digital input



In Figure 2, the digital input is guaranteed to be pulled high because of the 10k ohm resistor. This implementation would work on both the old and new design of the PIO-24 and is the preferred implementation to avoid dependence on a specific level of input load current.